REMARKS

In the non-final 18 January 2006 *Office Action*, the Examiner rejects Claims 1-22. Applicant thanks the Examiner with appreciation for the careful consideration and examination given to the Application.

After entry of this Response, Claims 1-22 are pending in the Application. Applicant respectfully asserts that Claims 1-22 are in condition for allowance and respectfully request reconsideration of the claims in light of the following remarks.

The undersigned respectfully requests a telephonic conference with the Examiner regarding the following remarks and the cited references.

I. Pending Claims & Present Invention

As the Examiner will recall, embodiments of Applicant's invention can provide a method of sparing and removing pinned or interleaved memory upon memory device failure in a memory system. When a memory device failure is predicted in a device containing pinned memory, a request can be made for the de-allocation of a freeable memory range. When the request for de-allocating the freeable range of memory is accepted, the stored memory in the failing memory device can be copied to one or more of the de-allocated memory devices. Requests directed to the failing memory device may be re-routed to one or more replacement memory devices. Also, after the stored memory is copied to a replacement memory, the memory system can be interleaved.

Applicant's currently pending claims recite various features directed toward a method of sparing memory devices containing pinned memory. As discussed in detail below, Applicant respectfully submits that the references of record do not render Applicant's claims unpatentable. Importantly, the cited references do not mention, discuss, disclose, or fairly suggest any methods or systems to spare pinned memory upon a memory device failure in an interleaved memory system. For example, the cited references specifically fail to disclose, teach, or suggest pinned memory being confined to a non-freeable range of a computer memory and copying pinned memory from a failing memory device to another memory device as claimed by Applicant. For at least these reasons and the below-discussed reasons, Applicant respectfully asserts that Claims 1-22 are patentable over the cited references.

II. 35 U.S.C. § 102 Rejection

The Examiner rejects Claims 1-8, 10-13, 16-17 and 19-20 under 35 U.S.C. § 102(e) as allegedly being anticipated by *Parrish* (USPN 5,117,350). The Examiner asserts that *Parrish* discloses the subject matter contained in Claims 1-8, 10-13, 16-17 and 19-20. Applicant respectfully traverses the § 102 rejection.

Parrish discloses a memory address mechanism in a distributed memory architecture. In short, *Parrish* teaches a method of connecting various nodes (computing devices) to allow the nodes to share memory resources using a three-tier memory addressing scheme. (Col. 8, Lines 46-57). As best illustrated in FIG. 7 of *Parrish* (shown below), Parrish's address mechanism enables multiple computing devices to share memory resources utilizing a system wide addressing scheme. (Col. 7, Lines 3-22). Indeed, a main objective of *Parrish* is to allow varying sizes of memory resources to be interconnected without being stifled by or limited by a small memory which hindered previous addressing efforts. (Col. 9, Lines 44-65). *Parrish* utilizes "partition RAM" tables to implement the three-tier memory addressing scheme.

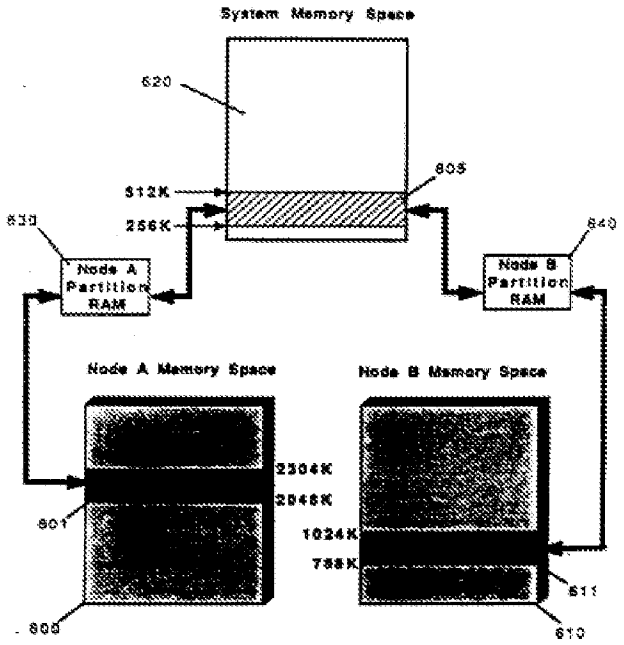

Figure 7

Parrish's partition RAM tables are software components that convert one memory location format to another memory location format. (Col. 9, Lines 25-43). Indeed, as illustrated in FIG. 7, the partition RAMs (630, 640) are shown between node memory spaces (A 600, B 610) and system memory space (620). The two node memory spaces include two local memory

partitions that are associated with the system memory space. (Col. 12, Lines 61-68). A write to one of the local memory partitions would eventually lead to the same data being written to the other local memory partitions so that computing devices at several nodes can share the same data and be updated simultaneously with greatly reduced bus traffic. (Col. 13, Lines 1-20). Thus, the *Parrish* distributed memory addressing scheme allows data to be copied from multiple memory locations residing on different networked nodes to other networked nodes.

Importantly, however, *Parrish* does not teach or suggest several features and limitations appearing in Applicant's claims. Notably, *Parrish* lacks any discussion of moving stored memory from a failing memory device as claimed by Applicant. Further, *Parrish* is not even remotely closely related to solving the problems solved by Applicant's claimed invention, which includes moving data to an operational memory device upon the failure of another memory device.

Parrish also fails to teach other features and limitation claimed by Applicant. For example, *Parrish* is silent on pinned memory, having pinned memory within the non-freeable range of a memory, and moving pinned memory to another memory device as claimed in independent Claims 1, 13, and 19. Indeed, the portions of *Parrish* cited in the *Office Action* as disclosing such features fail to teach pinned memory much less the other claimed features. For at least this reason, Claims 1, 13, and 19, and their respective dependent claims are allowable over *Parrish*.

Applicant respectfully asserts that the currently pending dependent claims are also allowable over *Parrish*. For example, Claims 6-9, 16, and 20 are not anticipated by *Parrish*. These claims include certain features relating to detection of memory device failure holding pinned memory and sparing the pinned memory to another memory device. Again, the portions of *Parrish* cited in the *Office Action* for disclosing these features do not anticipate Claims 6-9, 16, and 20. Take for example, portions of Column 18 cited as anticipating Claims 6-9. Nothing in Column 18 remotely discusses detecting memory device failure or how to detect memory device failure.

Column 18 does discuss a "create memory partition" procedure. This procedure "will first examine the system partition table to see if a partition of that name has already been created [and] whether there is enough room in the system address space to fit that size partition" as a result of a local partition being created. (Col. 16, Lines 47-58). As *Parrish* further explains, part

of the "create memory partition" procedure includes validating three parameters: partition identifier, partition type, and partition size. (Col. 18, Lines 6-12). If these three parameters are correct, a new memory partition is made otherwise an error message is returned. (Col. 18, Lines 12-28).

It is very important to note that *Parrish's* "create memory partition" procedure does not detect whether a memory device is failing. Applicant, however, claims such a feature in Claim 6. *Parrish* is also silent regarding what occurs when a memory device occurs and how a memory device is tested for failure. Again, Applicant claims such features in Claims 6-9.

Another dependent claim not anticipated by *Parrish* is Claim 16. The Examiner asserts that Col. 10, Lines 48-50 describe "memory invalidation and dirty memory." However, this portion of *Parrish* does not anticipate Claim 16 (i.e., it fails to disclose that the memory device containing pinned memory is failing). Rather, this portion of *Parrish* discusses and even defines that dirty cache memory is not updated cache. This portion of *Parrish* says nothing about a failing memory device.

For at least the above reasons, Applicant respectfully asserts that Applicant's currently claimed invention (Claims 1-22) is allowable over *Parrish*. Withdrawal of the § 102 rejection is respectfully requested.

III. 35 U.S.C. § 103 Rejections

The Examiner asserts that several claims are unpatentable under 35 U.S.C. § 103. Specifically, the Examiner asserts that: (1) a combination of *Parrish* and *Savage* (USPN 4,797,853) renders Claim 9 unpatentable; (2) a combination of *Parrish* and *Bauman* I (USPN 6,415,364) renders Claims 14 and 15 unpatentable; (3) a combination of *Parrish* and *Bauman* II (USPN 6,381,715) renders Claim 18 unpatentable; and (4) a combination of *Parrish* and *Tsang* (USPN 5,537,112) renders Claims 21 and 22 unpatentable.

Applicant respectfully traverses the § 103 rejections in light of the above-presented remarks regarding *Parrish*. Because *Parrish* fails to teach each and every claimed limitation of the independent claims as discussed above, the asserted § 103 rejections also fail to teach the subject matter as a whole as claimed in dependent Claims 9, 14-15, 18, and 21-22. Accordingly, Applicant respectfully asserts that Claims 9, 14-15, 18, and 21-22 are allowable over the cited combinations.

V. Fees

Applicant files this Response within three months of the 18 January 2006 Office Action and with no additional claims. Accordingly, Applicant believes that no extension or claims fees are due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507.

VI. Conclusion

The foregoing is believed to be a complete response to the non-final *Office Action* mailed 18 January 2006. Applicant respectfully asserts that Claims 1-22 are in condition for allowance and respectfully requests passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Hunter Yancey at (404) 885-3696 is respectfully requested.

Respectfully submitted,

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